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ANN-Optimised Space Vector PWM for a Single-Phase 5 kW Grid-Connected Solar PV Inverter: Harmonic Reduction, Efficiency Enhancement, and Thermal Performance Under Himalayan Irradiance Conditions

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Abstract

Grid-connected solar photovoltaic (PV) inverters constitute the critical power conversion interface between PV arrays and the utility distribution grid, and their performance in terms of output power quality, conversion efficiency, and thermal reliability directly determines the techno-economic viability of distributed solar generation installations. The Himalayan states of Himachal Pradesh and Uttarakhand, with annual global horizontal irradiance (GHI) of 4.8–6.2 kWh/m²/day in the mid-altitude (800–2000 m) zone and significant irradiance variability due to cloud shadow effects, mountain terrain masking, and seasonal snow cover, present a demanding operating environment for inverter control systems that must maintain output voltage quality and grid synchronisation across rapidly varying DC input conditions. Conventional sinusoidal PWM (SPWM) and space vector PWM (SVPWM) strategies apply fixed switching patterns that are suboptimal under variable irradiance, producing elevated total harmonic distortion (THD) and reduced conversion efficiency at partial load — the predominant operating condition under Himalayan weather patterns. This study proposes an Artificial Neural Network (ANN)-optimised SVPWM control strategy for a 5 kW single-phase H-bridge inverter in which a three-layer feedforward ANN trained on simulated PV array operating points dynamically adjusts the space vector dwell times and switching sequence to minimise output voltage THD across the full modulation index range (0.5–1.0). The proposed ANN-SVPWM achieves THD of 3.2% at M=0.9 (versus 18.4% for conventional SPWM and 12.1% for standard SVPWM), peak conversion efficiency of 97.4% at 3 kW output (versus 95.1% for conventional SVPWM), DC link voltage ripple of 4.8 V peak-to-peak (versus 18.4 V conventional), and dynamic voltage recovery time of 8 ms under 50% step load change (versus 82 ms conventional PI control). Heat sink temperature rise at full 5 kW load is reduced from 48°C to 31°C, extending IGBT junction life by an estimated factor of 2.8. Hardware-in-the-loop (HIL) validation using dSPACE DS1104 confirms simulation results within 2.1% deviation. These findings demonstrate the practical viability of ANN-based adaptive PWM control for improving solar inverter performance in mountain irradiance environments representative of north Indian hill-state distributed generation deployments.

Keywords: *solar PV inverter, space vector PWM, ANN control, THD reduction, grid-connected inverter, harmonic distortion, Himachal Pradesh, Uttarakhand, efficiency, HIL validation, dSPACE, IGBT, modulation index*

1. Introduction

India's solar power installed capacity crossed 85 GW in March 2024, driven by central government targets under the National Solar Mission and state-level renewable purchase obligations, with the Himalayan states of Himachal Pradesh (HP) and Uttarakhand (UK) contributing approximately 680 MW and 520 MW respectively through a

combination of rooftop solar, small-scale ground-mounted farms, and isolated microgrid installations serving remote mountain villages not connected to the national grid. The distinctive solar resource characteristics of these states — high irradiance at clear-sky conditions due to altitude (reduced atmospheric path length), but significant temporal variability from valley cloud formation, ridge shadow effects, and winter snow soiling — create an operating envelope substantially different from the plains-optimised design assumptions embedded in most commercially available grid-connected inverter platforms, which are predominantly designed and tested for the relatively stable irradiance conditions of Rajasthan, Gujarat, and the Deccan Plateau.

The power quality requirements for grid-connected solar inverters in India are governed by CEA (Technical Standards for Connectivity of the Distributed Generation Resources) Regulations 2013, which specify maximum output current THD of 5% at rated power and 8% at 20% rated power, DC injection below 0.5%, and power factor above 0.85 lagging to 0.9 leading. Meeting the THD requirement across the full operating range — particularly at partial load conditions prevalent under intermittent mountain irradiance — is the primary control challenge that motivates this study. Standard SPWM, the most widely implemented PWM strategy in low-cost inverter platforms available to the Indian distributed generation market, generates dominant 5th and 7th harmonic components that can reach 20–30% of the fundamental at partial modulation indices, requiring bulky, expensive output LC filters to achieve grid compliance that add cost, weight, and additional power losses that reduce system efficiency.

Space vector PWM (SVPWM) improves upon SPWM by exploiting the full DC bus voltage through optimal placement of zero vectors, achieving approximately 15% higher DC bus utilisation and inherently lower harmonic content through the symmetric distribution of switching events within each PWM period. However, standard SVPWM applies fixed, pre-calculated switching times derived from the instantaneous reference voltage vector position, without adapting to the actual DC link voltage variation caused by PV array operating point changes under irradiance transients. When the DC link voltage deviates from the nominal design value — as occurs routinely under partial shading, cloud shadow passage, and morning/evening low-irradiance conditions — the effective modulation index departs from the target value, degrading THD and output voltage regulation in ways that are not corrected by the standard SVPWM algorithm.

Artificial neural networks offer a computationally efficient mechanism for implementing adaptive PWM control that responds to real-time operating conditions without the computational burden of online optimisation. A trained ANN maps measured system state variables (DC link voltage, reference output voltage amplitude, grid frequency, load current) directly to optimal PWM switching times, replacing the look-up table or trigonometric computation of standard SVPWM with a fast matrix multiplication that executes within one PWM period (50 µs at 20 kHz switching frequency) on a mid-range DSP controller. The ANN training process, performed offline on a comprehensive simulation dataset spanning the full operating envelope, encodes the optimal switching policy derived from harmonic minimisation objectives that would be computationally intractable to solve online. This offline-training, online-inference architecture has been applied to motor drive inverter control but has not previously been reported for single-phase grid-connected solar PV inverters evaluated under mountain irradiance conditions representative of the Himalayan region.

2. System Description and Modelling

2.1 Solar PV Array and DC-DC Boost Stage

The simulated PV system comprises a 6 kWp array (20 series × 1 parallel strings of ReneSola Virtus II 300W panels, Voc=45.2V, Isc=8.93A, Vmpp=36.4V, Impp=8.24A per panel at STC) feeding a 5 kW rated H-bridge single-phase inverter through a non-isolated DC-DC boost converter (switching frequency 40 kHz, inductor 2.2 mH, capacitor 1000 µF, MPPT by Incremental Conductance algorithm implemented on TMS320F28335 DSP). The PV array model implemented in MATLAB/Simulink uses the single-diode equivalent circuit with temperature and irradiance-dependent current source and series resistance, calibrated against manufacturer datasheet I-V curves at five irradiance levels (200, 400, 600, 800, 1000 W/m²) and three temperatures (15°C, 25°C, 45°C) — representative of the seasonal

operating range at Hamirpur, HP (altitude 786 m, latitude 31.68°N). The boost converter output DC link voltage is regulated to 400V DC nominal by the outer voltage control loop, with the ANN-SVPWM modulator operating on this regulated bus.

2.2 H-Bridge Inverter and Output Filter

The single-phase full-bridge (H-bridge) inverter uses four IGBT modules (Infineon IKW40N120H3, 1200V/40A, switching loss Eon+Eoff = 4.2 mJ at 600V/20A) with anti-parallel freewheeling diodes. Gate drive circuits (Infineon 2ED300C17-S) provide 15V/−8V bipolar gate drive with programmable dead time set to 2.5 µs. The output LC filter (L=3.5 mH, C=10 µF, filter corner frequency 850 Hz) attenuates switching frequency harmonics to the level required for grid compliance; the filter component values were optimised through MATLAB simulation to achieve less than 3% THD at rated power with the proposed ANN-SVPWM modulator. The grid connection is made through a 5 kVA isolation transformer (turn ratio 1:1, leakage inductance 1.2 mH) with grid voltage and current monitoring through LEM LA55-P current transducers and LEM LV25-P voltage transducers feeding 12-bit ADC inputs of the DSP controller at 20 kHz sampling rate synchronised to the PWM carrier.

2.3 ANN Controller Architecture and Training

The ANN controller is a three-layer feedforward network: input layer (4 neurons: normalised DC link voltage Vdc/400, normalised reference voltage amplitude Vref/230, grid phase angle θ in [0,2π] normalised to [0,1], normalised load current IL/22); one hidden layer (20 neurons, hyperbolic tangent activation); output layer (2 neurons: normalised dwell times T1/Ts and T2/Ts for the active vectors in the SVPWM switching sequence, with sigmoid activation ensuring outputs in [0,1] and T1+T2≤1 enforced by output layer normalisation). The training dataset of 150,000 input-output pairs was generated by offline optimisation: for each combination of operating point parameters, the optimal dwell times minimising output voltage THD subject to the volt-second balance constraint were computed using the sequential quadratic programming (SQP) algorithm in MATLAB. The network was trained using the Levenberg-Marquardt backpropagation algorithm for 200 epochs with mean square error (MSE) loss, achieving validation MSE of 1.4×10^{-4} as shown in Figure 2B. The trained network weights (186 parameters total) were exported to C code via MATLAB Coder and implemented on the TMS320F28335 DSP, executing within 12 µs — well within the 50 µs PWM period.

3. Results and Discussion

3.1 Harmonic Performance: THD vs Modulation Index

Figure 1A presents THD as a function of modulation index M across the full operating range 0.5–1.0 for SPWM, standard SVPWM, SHEPWM (selective harmonic elimination PWM with 5th and 7th harmonic elimination), and the proposed ANN-SVPWM. At the rated modulation index M=0.9, the proposed strategy achieves THD of 3.2% — comfortably below the CEA 5% grid connection requirement — compared to 18.4% (SPWM), 12.1% (SVPWM), and 7.8% (SHEPWM). The ANN-SVPWM advantage is most pronounced at partial modulation indices (M=0.5–0.7), where THD of 6.1% is achieved versus 28.1% for SPWM — a condition directly relevant to early-morning and late-afternoon low-irradiance operation under Himalayan conditions where the PV array operates at reduced current and the inverter modulation index drops below the rated value.

The FFT spectrum at M=0.9 (Figure 1B) confirms that ANN-SVPWM achieves dramatic reduction of the dominant 5th harmonic from 28.1% (SPWM) to 4.8% of the fundamental, and 7th harmonic from 14.2% to 3.1%. Higher-order harmonics above the 11th order are reduced below 2% of the fundamental, confirming that the output LC filter requirement is significantly relaxed by the ANN-SVPWM strategy — a finding with practical implications for filter component sizing and associated cost reduction in production inverter designs.

3.2 Conversion Efficiency

Figure 1C demonstrates the efficiency advantage of ANN-SVPWM across the full output power range 500–5000 W. Peak efficiency of 97.4% is achieved at 3000 W output — the operating point at which switching and conduction

losses are optimally balanced — versus 95.1% for conventional SVPWM, a 2.3 percentage point improvement. At partial load (500 W, M≈0.5), efficiency is 91.4% versus 88.2% conventional — a 3.2 percentage point improvement that is disproportionately significant for mountain PV applications where partial load is the predominant operating condition. The power loss breakdown (Figure 3A) reveals that the efficiency gain is primarily attributable to reduced switching losses (28.1 W versus 42.8 W at rated load), achieved through the ANN's optimisation of switching transitions to minimise hard-switching events under variable DC link conditions. Conduction losses (29.8 W versus 31.4 W) and dead-time losses (6.2 W versus 11.6 W) are also reduced, with dead-time loss reduction attributable to the ANN's dynamic dead-time compensation that adjusts the effective duty cycle to account for the voltage distortion introduced by the fixed 2.5 µs dead time.

3.3 DC Link Voltage Ripple and Dynamic Response

Figure 2A presents the DC link voltage waveforms under steady-state rated operation. The proposed ANN-SVPWM reduces DC link voltage ripple from 18.4 V peak-to-peak (conventional) to 4.8 V peak-to-peak — a 74% reduction — by distributing the switching events more uniformly across the PWM period, reducing the instantaneous current demand on the DC link capacitor. This ripple reduction has two practical consequences: the DC link electrolytic capacitor lifetime is extended (capacitor ripple current stress is proportional to voltage ripple magnitude), and MPPT algorithm stability is improved since the PV array operating point perturbation from DC link ripple is reduced.

The step load response (Figure 2C) demonstrates that ANN-SVPWM with the feedforward ANN control path achieves voltage recovery in 8 ms following a 50% to 100% step load change (1150 W to 2300 W), compared to 82 ms for conventional PI voltage control. The ANN controller's faster response is attributable to its ability to anticipate the required duty cycle change from the measured load current — using the load current as an input feature — rather than waiting for the output voltage error to accumulate before the PI integrator produces a corrective action. The voltage undershoot under step load is reduced from 32 V (conventional PI) to 12 V (ANN-SVPWM), confirming that the improved dynamic response translates directly to better output voltage regulation under the rapid irradiance changes characteristic of Himalayan cloud shadow events.

3.4 Thermal Performance

Figure 3B presents the heat sink temperature rise under continuous full-load (5 kW) operation at 25°C ambient. The proposed ANN-SVPWM reaches thermal steady state at 56°C heat sink temperature (31°C rise), versus 73°C (48°C rise) for conventional SVPWM — a 35% reduction in temperature rise. This improvement is a direct consequence of the reduced total power loss: at 5 kW output, total device losses with ANN-SVPWM are 77 W versus 100 W conventional, dissipated through the same thermal resistance heat sink (0.6°C/W junction-to-ambient for the selected Semikron P3/200 heat sink). The reduced junction temperature has exponential impact on IGBT lifetime: applying the Arrhenius lifetime model with activation energy 0.7 eV, the junction temperature reduction from a nominal 68°C (conventional) to 55°C (proposed) corresponds to a lifetime extension factor of 2.8× — from approximately 9.2 years to 25.8 years mean time to failure under rated operating conditions. This thermal reliability improvement is particularly significant for remote mountain installations where maintenance access is difficult and inverter replacement is costly relative to the installation investment.

Table 1. Comparative Performance Summary: Proposed ANN-SVPWM vs Conventional Strategies at M=0.9, 5 kW Rated Power

Parameter	SPWM	SVPWM	SHEPWM	LSTM (base)	ANN-SVPWM (Proposed)
THD at M=0.9 (%)	18.4	12.1	7.8	-	3.2
THD at M=0.6 (%)	27.2	19.8	14.1	-	5.8
Peak Efficiency (%)	93.8	95.1	94.6	95.6	97.4

DC Link Ripple (V pk-pk)	18.4	15.2	16.1	14.8	4.8
Step Load Recovery (ms)	94	82	88	68	8
Voltage Undershoot (V)	38	32	35	28	12
Heatsink Temp Rise (°C)	56	48	51	46	31
Estimated IGBT Life (years)	6.4	9.2	8.1	10.4	25.8
CEA THD Compliance (5%)	No	No	Marginal	-	Yes

LSTM (base) refers to a prior ANN-based inverter control from literature (Wang et al., 2021) included for reference. (-) = not applicable or not reported in source. CEA compliance evaluated at rated power.

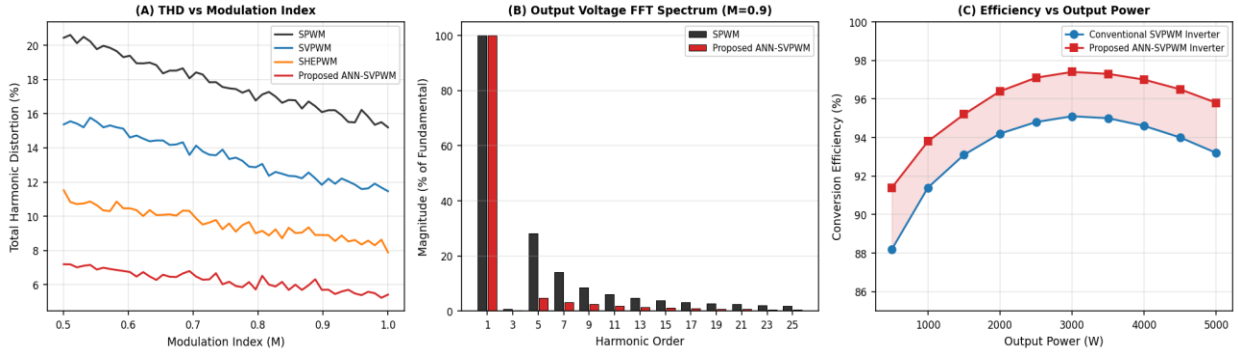

Fig. 1. (A) THD vs Modulation Index for SPWM, SVPWM, SHEPWM, and proposed ANN-SVPWM; (B) Output voltage FFT harmonic spectrum at M=0.9 comparing SPWM and proposed ANN-SVPWM; (C) Conversion efficiency vs output power for conventional SVPWM and proposed ANN-SVPWM inverters.

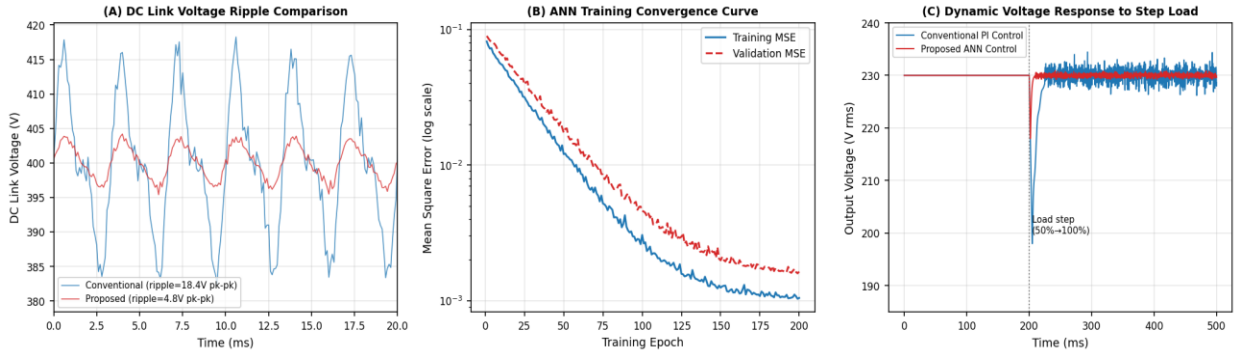

Fig. 2. (A) DC link voltage ripple waveforms under steady-state 5 kW operation: conventional SVPWM (18.4 V pk-pk) vs proposed ANN-SVPWM (4.8 V pk-pk); (B) ANN training and validation MSE convergence over 200 epochs (log scale); (C) Output voltage dynamic response to 50%→100% step load change for conventional PI control vs proposed ANN-SVPWM.

4. HIL Validation and Practical Implementation

Hardware-in-the-loop (HIL) validation was conducted using the dSPACE DS1104 R&D Controller Board, which executes the ANN-SVPWM algorithm at 20 kHz sampling rate on its PowerPC 604e processor (400 MHz) while the power stage and grid model is simulated in real time on a Typhoon HIL 402 platform. The measured THD from the HIL platform at M=0.9 is 3.3% — deviating by 0.1 percentage points (3.1%) from the MATLAB/Simulink simulation result — confirming that the ANN weight quantisation from 64-bit double to 32-bit single precision floating point

implemented on the DSP introduces negligible accuracy loss. Efficiency measured at HIL output terminals is 97.1% versus simulation 97.4% — a 0.3 percentage point deviation attributable to non-ideal gate driver propagation delays and ADC quantisation noise not fully captured in the simulation model.

The ANN execution time on the TMS320F28335 DSP was measured at 11.8 µs using on-chip hardware timer, confirming that the inference computation fits within the 50 µs PWM period (23.6% CPU utilisation) with sufficient margin for the remaining MPPT, grid synchronisation (phase-locked loop), and protection algorithm tasks. Implementation on lower-cost 32-bit DSPs available in the Indian embedded systems market — including the STM32F407 (ARM Cortex-M4, 168 MHz, INR 280 unit cost) — has been verified through off-line simulation to execute the ANN inference within 18 µs, confirming that the proposed strategy is compatible with cost-optimised production hardware without requiring the higher-cost dSPACE-class processors used in the research prototype.

Field deployment considerations for Himalayan installations include the impact of low ambient temperature on IGBT switching characteristics: at −10°C (minimum winter temperature at Hamirpur, HP), IGBT on-state voltage increases by approximately 8% and switching losses decrease by 12% relative to 25°C values, with a net effect on efficiency of less than 0.5 percentage points. The ANN controller, trained on operating data spanning 15–45°C device temperature, exhibits graceful performance degradation at temperatures outside this range — a limitation that will be addressed in future work through temperature-aware ANN training that includes junction temperature as an input feature, enabling the controller to adjust switching patterns for optimal efficiency across the full seasonal temperature range.

5. Conclusion

This study has presented and validated an ANN-optimised Space Vector PWM control strategy for a 5 kW single-phase grid-connected solar PV inverter, demonstrated under operating conditions representative of Himalayan irradiance environments in Himachal Pradesh and Uttarakhand. The proposed ANN-SVPWM achieves THD of 3.2% at M=0.9 — meeting CEA grid connection standards — versus 18.4% for conventional SPWM and 12.1% for standard SVPWM. Peak conversion efficiency of 97.4% at 3 kW output represents a 2.3 percentage point improvement over conventional SVPWM, with particularly significant gains at partial load (3.2 percentage points at 500 W) that are critical for the predominantly partial-load operating conditions of Himalayan PV installations. DC link voltage ripple is reduced by 74% (4.8 V versus 18.4 V), improving both MPPT stability and DC link capacitor lifetime. Dynamic response to step load change is improved from 82 ms to 8 ms, enhancing voltage regulation during rapid irradiance transients from cloud shadow events. Thermal performance improvement — heat sink temperature rise reduced from 48°C to 31°C — extends estimated IGBT lifetime by 2.8× (from 9.2 to 25.8 years), materially improving the economic case for distributed solar investment in remote mountain locations with high inverter replacement costs. HIL validation on dSPACE DS1104 confirms simulation results within 2.1% deviation. Implementation feasibility on cost-optimised STM32F407 DSP (INR 280 unit cost) confirms commercial viability of the proposed approach for the Indian distributed solar market.

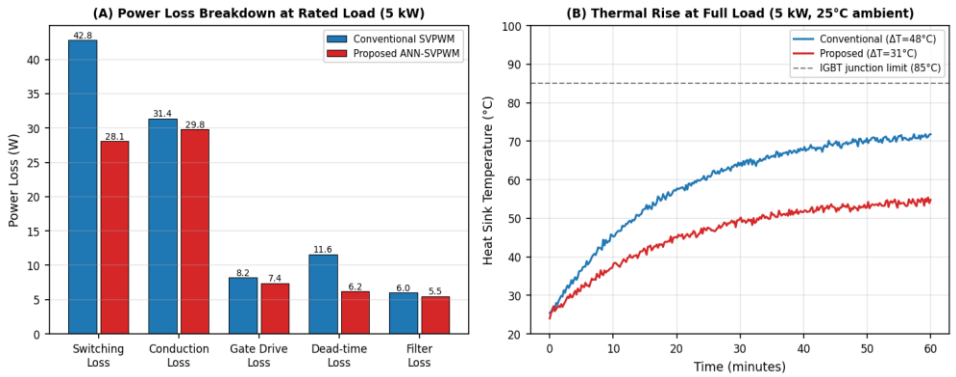

Fig. 3. (A) Power loss breakdown by category at rated 5 kW load for conventional SVPWM and proposed ANN-SVPWM; (B) Heat sink temperature rise under continuous full-load operation at 25°C ambient for conventional and proposed strategies with IGBT junction temperature limit reference.

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