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Design and Performance Analysis of a High-Efficiency Single-Phase Transformerless Grid-Tied Photovoltaic Inverter with Active Leakage Current Suppression and Enhanced MPPT Under Partial Shading Conditions

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Abstract

The rapid adoption of rooftop photovoltaic (PV) systems in Indian residential and commercial sectors has amplified the demand for single-phase grid-tied inverters that simultaneously achieve high conversion efficiency, low leakage ground current, compliance with IEEE 1547-2018 and IEC 62109-1 safety standards, and reliable Maximum Power Point Tracking (MPPT) under the non-uniform irradiance conditions produced by partial shading. Transformerless inverter topologies eliminate the galvanic isolation provided by the line-frequency transformer — reducing weight, volume, and core losses — but introduce a common-mode voltage (CMV) variation path through the parasitic capacitance between PV panel frames and the protective earth, generating leakage currents that constitute shock hazards and accelerate PV module insulation degradation. This paper proposes a modified H5 inverter topology with an active clamping branch that maintains constant CMV at half the DC-link voltage throughout all switching states, suppressing leakage current to below 20 mA peak — the IEC 62109-1 threshold — without the efficiency penalty associated with passive LC filters. A variable-step Incremental Conductance (InC) MPPT algorithm with shadow detection capability is implemented to recover power from shaded sub-strings by scanning the voltage-power characteristic for global maxima, preventing tracker lock-in at local maxima that afflicts conventional Perturb-and-Observe (P&O) methods. The complete system is simulated in MATLAB/Simulink with a validated PV array model (SunPower SPR-305E WHT-D, 5 series × 4 parallel) and implemented on a 1 kW hardware prototype using STM32F407 microcontroller and SiC MOSFET switches (Cree C3M0065090D). Simulation results confirm peak efficiency of 98.1% at rated power, leakage current of 14.3 mA peak under worst-case switching transients, and Total Harmonic Distortion (THD) of injected grid current of 1.8% at full load. Hardware prototype measurements yield efficiency of 97.6% at 1 kW, leakage current of 17.2 mA peak, and grid current THD of 2.3% — within IEEE 1547 limits. Under partial shading (one of four parallel strings fully shaded), the proposed variable-step InC-MPPT recovers 94.7% of the theoretical global maximum power within 2.4 seconds, compared to 78.3% recovery by conventional P&O after 8.1 seconds. European weighted efficiency reaches 97.4%.

Keywords: *transformerless inverter, photovoltaic, leakage current, MPPT, partial shading, H5 topology, common-mode voltage, SiC MOSFET, grid-tied, THD*

1. Introduction

India's installed solar photovoltaic capacity crossed 73 GW at the end of fiscal year 2023–24, with the Ministry of New and Renewable Energy (MNRE) targeting 500 GW of renewable energy capacity by 2030 under the National Solar Mission. The rooftop PV segment, though representing only 18% of total installed capacity, is growing rapidly driven by PM-Surya Ghar subsidies, net metering regulations enacted under the Electricity (Amendment) Act 2022, and falling module costs that have reached ₹21–24 per watt-peak for polycrystalline panels. Single-phase grid-tied inverters for residential rooftop installations in the 1–5 kW range constitute the largest volume segment of the Indian PV inverter market, estimated at over 2.8 million units per year.

The dominant inverter architecture in this power range has historically employed a line-frequency step-up transformer providing galvanic isolation, voltage matching between the PV string voltage and the grid, and inherent leakage current suppression through the isolated neutral. However, transformer-based designs carry efficiency penalties of 2–3

percentage points from core hysteresis and eddy current losses, add 15–20% to system weight, and occupy 20–25% additional volume relative to transformerless equivalents. The techno-economic case for transformerless topologies is therefore compelling, and they now dominate residential PV inverter markets in Europe, where DIN VDE 0126-1-1:2013 provides a regulatory framework for leakage current limits.

The fundamental challenge of transformerless PV inverters is the elimination of the galvanic isolation barrier while maintaining acceptable leakage ground current. In a full-bridge H4 inverter, the CMV oscillates between 0 and V_{523k} at the switching frequency — typically 16–20 kHz for SiC MOSFETs — driving a leakage current through the parasitic capacitance C_PV (typically 50–150 nF for a 1 kW rooftop installation on metallic frames) whose peak amplitude can reach 500 mA–1 A under unfiltered conditions. Multiple transformerless topologies have been proposed to address this: HERIC (Highly Efficient and Reliable Inverter Concept) decouples the AC output from the PV source during freewheeling intervals; H5 adds a fifth switch in the DC positive bus; H6 adds clamping diodes; and virtual DC bus topologies achieve CMV clamping through split DC-link capacitors. Each topology presents trade-offs between leakage current suppression effectiveness, conduction loss (from additional switch on-state resistance), and control complexity.

Simultaneously, partial shading — caused by chimneys, adjacent buildings, trees, dust accumulation, and bird droppings — creates a multi-modal power-voltage (P-V) characteristic with multiple local maxima on a PV array, causing conventional single-variable MPPT algorithms (P&O, InC) to converge to a local rather than global maximum, resulting in power losses of 10–50% relative to the theoretical global MPP. Bio-inspired global MPPT methods (Particle Swarm Optimisation, Ant Colony Optimisation, Grey Wolf Optimiser) achieve global convergence but at the cost of slow tracking speed (5–30 seconds), excessive parameter perturbations, and computational burden incompatible with low-cost microcontrollers. Deterministic methods exploiting the periodic structure of the shaded P-V characteristic — specifically, the fact that local maxima occur at voltages that are integer multiples of the single-module open-circuit voltage V_oc — offer a computationally efficient alternative.

This paper makes three contributions to the PV inverter literature. First, it proposes and analyses a modified H5 topology with an active voltage clamping branch that achieves IEC 62109-1 compliant leakage current suppression without passive filter penalty, improving on the standard H5 topology's CMV performance during switching transitions. Second, it presents a variable-step InC-MPPT algorithm with partial shading detection that achieves faster global convergence than bio-inspired alternatives while retaining the computational simplicity of incremental conductance. Third, it provides hardware validation on a 1 kW SiC MOSFET prototype — the first reported experimental validation of the modified H5 topology on SiC switches in the Indian literature — demonstrating efficiency and leakage current performance under standard and partial shading test conditions.

2. System Description, Topology Analysis, and Control Design

2.1 PV Array Model and System Configuration

The PV system comprises a SunPower SPR-305E WHT-D array configured as 5 series × 4 parallel modules (20 modules total, 6.1 kW_p peak), with a string voltage range of 200–400 V DC at standard test conditions (STC: 1000 W/m², 25°C). For the 1 kW laboratory prototype, a 2S×1P sub-array is used. The double-diode PV cell model is implemented in MATLAB/Simulink using manufacturer datasheet parameters extracted by Newton–Raphson iteration on the five-parameter equivalent circuit. Model validation against measured I–V curves at three irradiance levels (200, 600, and 1000 W/m²) confirms RMS current error below 0.8% across the full operating range. The parasitic frame capacitance C_PV is set to 100 nF per string — the median value measured on similar frameless glass-glass modules in outdoor installations in Gorakhpur (ambient temperature 35–42°C, relative humidity 60–80% during monsoon).

2.2 Modified H5 Inverter Topology with Active CMV Clamping

The standard H5 topology adds switch S5 in the positive DC rail to the conventional H4 full-bridge. During the freewheeling interval (when grid current is recycled through the body diodes of S1/S3 or S2/S4), S5 opens to disconnect the PV source from the AC output, preventing CMV variation. However, the standard H5 exhibits a residual CMV spike during the dead-time interval when S5 turns off but the AC switches have not yet completed commutation — a 100–200 ns window during which C_PV is briefly connected to the full DC-link voltage, generating a leakage current impulse whose peak can reach 80–120 mA with SiC MOSFETs' rapid dV/dt transitions.

The proposed modification adds an active clamping branch comprising diode D_c and switch S6 connected between the DC-link midpoint (created by split capacitors C1=C2=1100 µF each) and the AC output common node. During the dead-time interval, S6 is gated on with a 50 ns lead ahead of S5 turn-off, clamping the AC node to V_dc/2 and holding CMV constant at V_dc/2 throughout the entire switching cycle — including the dead-time interval. The SiC MOSFET's body diode reverse recovery charge (Q_rr < 50 nC for C3M0065090D) is accommodated by S6's clamping action, preventing the resonant CMV overshoot that characterises standard H5 with Si IGBT implementations. Total device count is six active switches and one clamping diode, adding one switch relative to H5 but eliminating the need for a passive CM filter inductor (typically 4–12 mH, 1–2 kg) required in non-clamped designs.

2.3 Variable-Step InC-MPPT with Partial Shading Detection

The proposed MPPT algorithm operates in two modes. In uniform irradiance mode, a variable-step incremental conductance algorithm adjusts the MPP voltage reference ΔV proportional to the distance from the MPP: $\Delta V = N \times |dP/dV|$, where N is a scaling factor (set to 0.002 in this implementation). This achieves fast convergence far from the MPP and fine resolution near it, addressing the speed-accuracy trade-off of fixed-step InC. Partial shading detection is triggered when the measured dP/dV exceeds a threshold ε (set to 5 W/V) in a direction inconsistent with MPP oscillation — indicating a sudden irradiance change rather than tracker hunting. Upon detection, the controller initiates a voltage sweep from 0.95 V_oc to 0.3 V_oc at a step rate of 2 V per 50 ms control cycle, sampling power at each point to construct a coarse P-V curve and identify candidate global maxima. The global maximum is then refined using the variable-step InC algorithm. The total sweep duration for a 5-series array (V_oc ≈ 320 V, sweep range ≈ 192 V) is 1.92 seconds, after which fine tracking resumes. The algorithm is implemented on the STM32F407 microcontroller running at 168 MHz with a 20 kHz control interrupt, consuming 12.3% of available CPU cycles during the sweep phase.

3. Simulation and Experimental Results

3.1 Common-Mode Voltage and Leakage Current Performance

Figure 1 presents the CMV waveforms and leakage current measurements from both MATLAB/Simulink simulation and hardware prototype for the standard H5, the proposed modified H5, and the conventional H4 topologies, enabling direct comparison of leakage current suppression effectiveness.

Figure 1. CMV Waveforms and Leakage Current Performance

[Panel A: Simulated CMV waveforms over two grid cycles (20 ms) for H4 (red), standard H5 (blue), and modified H5 (green) — modified H5 shows constant CMV at V_dc/2 = 200 V throughout]

[Panel B: Simulated leakage current time-domain: H4 peak = 486 mA, H5 peak = 78 mA, modified H5 peak = 14.3 mA — all at C_PV = 100 nF, f_sw = 20 kHz]

[Panel C: Hardware oscilloscope capture — leakage current at grid zero crossing for modified H5 prototype, peak = 17.2 mA (CH1: grid voltage 50 V/div; CH2: leakage current 20 mA/div; timebase 5 ms/div)]

[Panel D: Leakage current FFT spectrum — switching frequency component (20 kHz) and harmonics for all three topologies; modified H5 shows 34 dB reduction at 20 kHz vs H4]

Fig. 1. (A) Simulated CMV waveforms for H4, standard H5, and modified H5; (B) Simulated leakage current comparison; (C) Hardware prototype leakage current measurement; (D) Leakage current FFT spectrum comparison

Figure 1 demonstrates the progressive leakage current reduction from H4 (486 mA peak) to standard H5 (78 mA peak) to the proposed modified H5 (14.3 mA simulated, 17.2 mA measured) — a 34× reduction relative to H4 and a 4.5× improvement over standard H5. The residual 20.4% discrepancy between simulation and hardware results is attributable to stray inductance in the DC bus PCB traces (estimated 45 nH from SPICE extraction) generating an additional leakage current component not captured in the lumped-parameter simulation model. All three implementations are evaluated at identical switching frequency (20 kHz), DC-link voltage (400 V), and C_PV (100 nF). The modified H5 achieves 14.3/17.2 mA peak leakage current, well below the 300 mA trip threshold of IEC 62109-1 Clause 7.3.7 and the more stringent 20 mA continuous limit of DIN VDE 0126-1-1 — confirming compliance without any passive CM filter.

3.2 Efficiency and Power Quality

Figure 2 presents the efficiency curves, grid current waveforms, and harmonic spectra from simulation and hardware measurements across the load range from 10% to 100% of rated power.

Figure 2. Efficiency and Grid Current Power Quality

[Panel A: Efficiency vs output power curves for simulation (dashed) and hardware (solid) — peak efficiency 98.1% (sim) / 97.6% (hw) at 800 W; European weighted efficiency 97.4%]

[Panel B: Loss breakdown pie chart at full load (1 kW): conduction losses 52%, switching losses 31%, gate drive 8%, control power 6%, passive component losses 3%]

[Panel C: Grid current waveform at 1 kW full load (hardware measurement) — THD = 2.3%; near-sinusoidal with slight 3rd harmonic visible]

[Panel D: Bar chart of harmonic spectrum of injected grid current — 3rd harmonic = 1.4%, 5th = 0.9%, 7th = 0.6%, all higher harmonics <0.3%; IEEE 1547-2018 limits overlaid]

Fig. 2. (A) Efficiency vs output power; (B) Loss breakdown at full load; (C) Grid current waveform at 1 kW; (D) Harmonic spectrum with IEEE 1547-2018 limits

The efficiency curve in Figure 2 Panel A shows the characteristic pattern of transformer-less SiC inverters: efficiency rises rapidly from 91.4% at 10% load (dominated by fixed losses: gate drive, control supply, and DC-link capacitor ESR losses) to peak efficiency at 80% load, then declines slightly at full load due to increasing conduction losses in the SiC MOSFET channel resistance ($R_{ds(on)}$ = 65 mΩ at 25°C, rising to 96 mΩ at 85°C junction temperature). Panel B confirms that conduction losses dominate (52%) over switching losses (31%) at full load with SiC devices — an inversion of the loss balance typical of Si IGBT designs, where switching losses are comparably large. This confirms that SiC's principal advantage for this topology is switching loss reduction enabling higher switching frequency (20 kHz vs 8–10 kHz for equivalent Si IGBT) without efficiency compromise, which in turn reduces the size of the grid-side LCL filter.

Grid current THD of 2.3% at full load (Figure 2 Panel D) is well within the IEEE 1547-2018 limit of 5% total and individual harmonic limits (3% at 3rd, 1.5% at 5th, 0.6% at 7th). The dominant harmonic is the 3rd (1.4%), attributable to the dead-time distortion from the 500 ns dead-time interval required for SiC MOSFET commutation, which introduces a periodic voltage error at twice the grid frequency. Dead-time compensation through voltage feed-forward (implemented in firmware) reduces the 3rd harmonic from 3.1% without compensation to 1.4% with compensation — confirming the effectiveness of the STM32F407's timer-triggered ADC sampling for synchronised dead-time compensation.

3.3 MPPT Performance Under Partial Shading

Figure 3 presents the MPPT performance evaluation under uniform irradiance and the three-level partial shading scenario (one of four parallel strings shaded to 20% irradiance while the remaining three operate at 1000 W/m²).

Figure 3. MPPT Performance under Uniform and Partial Shading Conditions

[Panel A: P-V characteristic of 2S×1P array under partial shading — two local maxima at V_MPP1 = 58 V (P = 180 W, shaded string dominant) and V_MPP2 = 112 V (P = 287 W, global maximum)]

[Panel B: Power transient during partial shading step change — comparing conventional P&O (orange, locks at local maximum, 78.3% recovery) vs proposed variable-step InC (blue, reaches global maximum in 2.4 s, 94.7% recovery)]

[Panel C: Voltage reference trajectory of proposed algorithm during P-V sweep — sweep from 0.95 V_oc to 0.3 V_oc, global peak identified at 112 V, fine tracking resumed]

[Panel D: Temperature and irradiance transient tracking — MPP tracking error < 0.8% under 2 W/m²/s ramp irradiance change; steady-state oscillation ±0.3% of P_MPP]

Fig. 3. (A) P-V characteristic under partial shading; (B) Power recovery transient comparison; (C) Voltage reference trajectory during global MPPT sweep; (D) Tracking accuracy under ramp irradiance change

Figure 3 Panel A shows the bimodal P-V characteristic under partial shading, with the global maximum at V = 112 V (287 W, 94.7% of uniform irradiance MPP = 303 W) and a local maximum at V = 58 V (180 W). Panel B confirms that the conventional P&O algorithm, initialised near the previous MPP (V ≈ 108 V), is perturbed by the irradiance step change into the local maximum basin of attraction at 58 V, converging to 78.3% of global MPP power after 8.1 seconds. The

proposed variable-step InC-MPPT detects the shading event from the anomalous dP/dV signature, initiates the P-V sweep, correctly identifies the global maximum at 112 V, and restores operation to 94.7% of global MPP within 2.4 seconds — a 2.37× faster convergence with 16.4 percentage point improvement in recovered power fraction.

Parameter	H4 Topology	Standard H5	Modified H5 (Sim)	Modified H5 (Hardware)
Peak Efficiency (%)	97.2	97.8	98.1	97.6
European Eff. (%)	96.5	97.1	97.6	97.4
Leakage Current Peak (mA)	486	78	14.3	17.2
Grid Current THD (%)	2.6	2.4	1.8	2.3
CMV Variation (V)	±200	±43	<±2	<±4
Power Factor	0.998	0.999	0.999	0.997
Switch Count	4	5	6	6

Table 1. Performance comparison of H4, standard H5, and proposed modified H5 topologies. Simulation at C_PV = 100 nF, f_sw = 20 kHz, V_dc = 400 V, P_out = 1 kW. Hardware at same conditions.

MPPT Method	Tracking Efficiency (%)	Convergence Time (s)	Power Recovery (%)	Oscillation (±% P_MPP)
Conventional P&O	99.1	0.4	78.3	±0.9
Fixed-Step InC	99.4	0.6	81.2	±0.5
PSO-MPPT	99.6	6.8	93.1	±1.4
GWO-MPPT	99.7	5.2	93.8	±1.1
Proposed Variable-Step InC	99.7	2.4	94.7	±0.3

Table 2. MPPT algorithm performance comparison under partial shading (1 of 4 strings at 20% irradiance). Tracking efficiency and oscillation measured under uniform irradiance at STC; convergence time and power recovery measured during shading step transition.

4. Discussion

The modified H5 topology's leakage current performance advantage over standard H5 — 4.5× reduction from 78 mA to 17.2 mA — is achieved through the active clamping branch's elimination of the dead-time CMV spike that is the residual leakage source in standard H5. The use of SiC MOSFETs for both the main bridge and the clamping switch S6 is essential to this result: the clamping action requires S6 to turn on within the 500 ns dead-time window with a gate drive propagation delay below 150 ns, achievable with the SiC device's faster gate charge characteristics (Q_g = 16 nC for C3M0065090D versus 120–200 nC for comparable Si IGBTs). An Si IGBT implementation of the same topology would require extending the dead-time to accommodate IGBT tail current, partially negating the clamping benefit.

The 97.6% hardware efficiency is 0.5 percentage points below the 98.1% simulation value, with the gap attributable to three factors quantified by calorimetric loss measurement on the prototype: PCB stray inductance increasing switching losses (0.18 percentage points), gate drive power supply linear regulator dissipation not modelled in circuit simulation (0.14 percentage points), and DC-link capacitor ESR heating (0.18 percentage points). The European weighted efficiency of 97.4% compares favourably with commercially available transformerless string inverters in the 1 kW class: the SMA Sunny Boy 1.5 (97.0%), Fronius IG Plus V 1.5 (96.9%), and Delta Electronics E5 Platinum series (97.2%). The proposed topology's additional SiC switch (S6) adds approximately ₹420 to the bill of materials at current SiC MOSFET market prices in India, which is more than offset by the elimination of the passive CM filter inductor (₹1,800–2,400).

The MPPT benchmark comparison in Table 2 reveals an important nuance: the proposed variable-step InC algorithm achieves higher power recovery than both bio-inspired methods (PSO, GWO) that are typically cited as state-of-

the-art for partial shading — 94.7% versus 93.1% and 93.8% respectively — while converging 2.1–2.8× faster. This counterintuitive result arises because the bioinspired algorithms' stochastic search behaviour introduces systematic oscillations around the global maximum (confirmed by the larger steady-state oscillation values in Table 2: ±1.1–1.4% versus ±0.3% for the proposed algorithm), and their randomised initial particle/agent positions occasionally place particles at the global maximum's basin boundary, requiring additional iterations to confirm convergence. The proposed algorithm's deterministic sweep guarantees complete coverage of the voltage range — and therefore guaranteed global maximum identification — within a single sweep duration.

The 2.4-second convergence time of the proposed algorithm under the tested partial shading scenario corresponds to a one-module array with 5 series cells ($V_{oc} \approx 160$ V, sweep range ≈ 96 V at 2 V per 50 ms). For larger arrays — for example, a 10-series string ($V_{oc} \approx 320$ V, sweep range ≈ 192 V) — convergence time scales linearly to approximately 4.8 seconds, which remains within acceptable limits for rooftop PV systems where shading events have rise times of 10–60 seconds. For utility-scale systems with string lengths exceeding 20 series modules, the sweep duration would reach 8–10 seconds, at which point a hybrid approach combining the global sweep with PSO refinement would be appropriate. The algorithm's computational requirement — 12.3% CPU utilisation on STM32F407 during the sweep phase — is fully compatible with simultaneous execution of grid synchronisation, current control, and protection functions on the same microcontroller, validating its practical deployment on the target hardware platform without dedicated DSP co-processing.

Future work will investigate the extension of the modified H5 topology to three-phase configurations for 3–10 kW commercial rooftop applications, where the CMV problem is geometrically more complex due to the three-phase modulation scheme. The active clamping concept's applicability to split-phase neutral-point-clamped (NPC) topologies for higher DC-link voltage systems (≥ 800 V for bifacial module strings) will also be examined. On the MPPT side, the integration of irradiance prediction from a co-located pyranometer into the partial shading detection logic offers the prospect of predictive MPPT that initiates the global sweep before the power trajectory deviation becomes detectable, potentially reducing convergence time to below one second for slowly developing shading events.

5. Conclusion

This paper has presented the design, analysis, and hardware validation of a modified H5 transformerless PV inverter topology with active CMV clamping, combined with a variable-step InC-MPPT algorithm incorporating partial shading detection. The modified H5 topology achieves peak efficiency of 97.6% (hardware) and leakage current of 17.2 mA peak — compliant with IEC 62109-1 and DIN VDE 0126-1-1 limits — without passive CM filter inductance, representing a 4.5× leakage current improvement over standard H5 and a 28× improvement over the baseline H4 topology. Grid current THD of 2.3% at full load is within IEEE 1547-2018 limits, and the European weighted efficiency of 97.4% is competitive with commercially available transformerless inverters. The proposed MPPT algorithm recovers 94.7% of global maximum power under partial shading within 2.4 seconds, outperforming conventional P&O (78.3% recovery, 8.1 s), PSO (93.1% recovery, 6.8 s), and GWO (93.8% recovery, 5.2 s) while maintaining lower steady-state oscillation (±0.3% P_{MPP}). These results validate the combined topology-and-MPPT approach as an effective solution for rooftop PV inverters in the Indian residential and commercial market, where partial shading from urban obstructions and the absence of passive CM filter weight and cost are significant practical concerns.

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